

REMARKS

Claims 1-30 are pending in the Application.

Claims 1-30 stand rejected.

I. REJECTIONS UNDER 35 U.S.C. §102(b)

The Office Action has rejected claims 1-30 under 35 U.S.C. §102(b) as being anticipated by *So* (U.S. Patent No. 6,148,389). Applicants respectfully traverse.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Regarding claims 1, 11 and 21, Applicants respectfully assert that *So* does not disclose "reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores." The Office Action relies upon column 1, lines 44-50; column 2, lines 29-35 and Figure 21 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse and assert that *So* instead discloses a PC system that includes a main CPU microprocessor, a file-based operating system, and a DSP microprocessor arranged so that the DSP can execute main CPU operations during time intervals in which the main CPU is otherwise occupied. Column 1, lines 44-48. *So* further discloses an integrated circuit having a DSP core, an interface circuit including a master/slave bus interface and a translation circuit, and a memory circuit comprising FIFO function coupled to the master/slave bus interface and a RAM function coupled to the translation circuit, and the DSP core is coupled to the memory and interface circuit. Column 2, lines 29-35. There is no language in the cited passages that discloses reading a data structure. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory in a DSP processor core. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory in a DSP processor core in a complex

comprising a plurality of DSP processor cores. Thus, *So* does not disclose all of the limitations of claims 1, 11 and 21.

Furthermore, regarding claims 1, 11 and 21, Applicants respectfully assert that *So* does not disclose "wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core." The Office Action relies upon column 16, lines 8-18 and Figure 21 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse and assert that *So* instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. *So* further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, *So* discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses a data structure that comprises a source address. Neither is there any language in the cited passage that discloses a data structure that comprises a source address indicating an address of where data is stored in the local memory of a DSP processor core. Thus, *So* does not disclose all of the limitations of claims 1, 11 and 21.

Additionally, regarding claims 1, 11 and 21, Applicants respectfully assert that *So* does not disclose "wherein said first data structure further comprises an indication of a size of a block of memory." The Office Action relies upon the statement "regions cannot exceed 128KB" in Figure 25 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. This statement is related to the size limitations of the scatter locked regions in a destination data DMA transfer table structure. This is not the same as having a data structure, associated with a block of local memory in a DSP processor core, that includes an indication of a size of a block of memory. Thus, *So* does not disclose all of the limitations of claims 1, 11 and 21.

Furthermore, regarding claims 1, 11 and 21, Applicants respectfully assert that *So* does not disclose "wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core." The Office relies upon column 16, lines 8-18 and Figure 21 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. *So* further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, *So* discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses a data structure, associated with a block of local memory in a DSP processor core, that includes a destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core. Thus, *So* does not disclose all of the limitations of claims 1, 11 and 21.

Additionally, regarding claims 1, 11 and 21, Applicants respectfully assert that *So* does not disclose "initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse and assert that *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of moving data. Neither is there any language in the cited passage that discloses initiating a transfer of moving data the size of the block of memory located in the first source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of moving data the size of the block of

memory located in the first source address in the local memory of the first DSP processor core to the destination address in the local memory of the second DSP processor core. Thus, *So* does not disclose all of the limitations of claims 1, 11 and 21.

Regarding claims 2, 12 and 22, Applicants respectfully assert that *So* does not disclose "obtaining a pointer to a second data structure from said first data structure." The Office Action relies upon the statement of "linked list" in Figure 22 of *So* as disclosing the above-cited claim limitation. The Office Action further states that it is well known in the art for a linked list to include data structure entries which point from a preceding structure to a subsequent structure. Applicants respectfully traverse. A linked list is a group of items, each of which points to the next item. *See [www.techweb.com/encyclopedia](http://www.techweb.com/encyclopedia)*. However, there is no language in *So* that describes the linked list referred to in Figure 22 as disclosing the aspect of obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core. Instead, Figure 22 illustrates a table of region lists which are not data structures associated with local memories of DSP processor cores. Thus, *So* does not disclose all of the limitations of claims 2, 12 and 22.

Further, in connection with the rejection of the above-cited claim limitation, Applicants respectfully assert that the Office Action must provide a basis in fact and/or technical reasoning to support the assertion that *So* inherently discloses obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that *So* inherently discloses obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Office Action has not provided any such objective evidence, the Office Action has not presented a *prima facie* case of anticipation for rejecting claims 2, 12 and 22.

Regarding claims 2, 12 and 22, Applicants respectfully assert that *So* does not disclose "reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer." The Office Action relied upon column 16, lines 8-18 and Figure 21 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. *So* further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, *So* discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses reading a second data structure. Neither is there any language in the cited passage that discloses reading a second data structure, where the second data structure includes a second source address of one of a read pointer and a write pointer. Neither is there any language in the cited passage that discloses reading a second data structure, where the second data structure includes a second destination address of one of the read pointer and the write pointer. Thus, *So* does not disclose all of the limitations of claims 2, 12 and 22.

Regarding claims 3, 13 and 23, Applicants respectfully assert that *So* does not disclose "initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that disclose initiating a transfer of a write pointer located in a second source

address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a write pointer located in a second source address in the local memory of the first DSP processor core to the second destination address in the local memory of the second DSP processor core. Thus, *So* does not disclose all of the limitations of claims 3, 13 and 23.

Regarding claims 4, 14 and 24, Applicants respectfully assert that *So* does not disclose "initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of a read pointer located in the second source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a read pointer located in the second source address in the local memory of the second DSP processor core to the second destination address in the local memory of the first DSP processor core. Thus, *So* does not disclose all of the limitations of claims 4, 14 and 24.

Regarding claims 5, 15 and 25, Applicants respectfully assert that *So* does not disclose "obtaining a pointer to a third data structure from said second data structure." The Office Action relies upon the statement of "linked list" in Figure 22 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. The Office Action must provide a basis in fact and/or technical reasoning to support the assertion that the statement of "linked list" in Figure 22 of *So* inherently discloses obtaining a pointer to a third data structure from a second data structure. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the

Examiner must provide extrinsic evidence that must make clear that the statement of "linked list" in Figure 22 of *So* inherently discloses obtaining a pointer to a third data structure from a second data structure, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Office Action has not provided any such objective evidence, the Office Action has not presented a *prima facie* case of anticipation for rejecting claims 5, 15 and 25.

Regarding claims 5, 15 and 25, Applicants respectfully assert that *So* does not disclose "reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer." The Office Action relies upon column 16, lines 8-18 and Figure 21 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. *So* further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, *So* discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses reading a third data structure. Neither is there any language in the cited passage that discloses reading a third data structure, where the third data structure includes a third source address of one of a read pointer and a write pointer. Neither is there any language in the cited passage that discloses reading a third data structure, where the third data structure includes a third destination address of one of the read pointer and the write pointer. Thus, *So* does not disclose all of the limitations of claims 5, 15 and 25.

Regarding claims 6, 16 and 26, Applicants respectfully assert that *So* does not disclose "initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said third source address in said

local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of a write pointer located in the second source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a write pointer located in the second source address in the local memory of the first DSP processor core to the second destination address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the third source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the third source address in the local memory of the second DSP processor core to the third destination address in the local memory of the first DSP processor core. Thus, *So* does not disclose all of the limitations of claims 6, 16 and 26.

Regarding claims 7, 17 and 27, Applicants respectfully assert that *So* does not disclose "initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to

locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of the write pointer located in the third source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the write pointer located in the third source address in the local memory of the first DSP processor core to the third destination address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the second source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the second source address in the local memory of the second DSP processor core to the second destination address in the local memory of the first DSP processor core. Thus, *So* does not disclose all of the limitations of claims 7, 17 and 27.

Regarding claims 8, 18 and 28, Applicants respectfully assert that *So* does not disclose "converting a local address of said write pointer to a global address." The Office Action relies upon column 19, lines 1-11 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse and assert that *So* instead discloses that the PCI address offset is the address in DSP space which will be translated into PCI space and used to transfer data from or to the host. Column 19, lines 1-3. There is no language in the cited passage that discloses converting a local address of the writer pointer (contained in the second data structure) to a global address. Thus, *So* does not disclose all of the limitations of claims 8, 18 and 28.

Regarding claims 8, 18 and 28, Applicants respectfully assert that *So* does not disclose "computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer." The Office Action relies upon column 23, lines 1-7 and 23-24 of *So* as well as Figure 24 as disclosing the above-cited claim limitation. Applicants respectfully traverse and assert that *So* instead discloses that for every transaction there is also known where the source and destination table is. Column 23, lines 1-2. *So* further discloses that Figure 24 is a detail of a region list for

the source data DMA transfer table. Column 23, lines 23-24. There is no language in the cited passages that discloses computing the first source address in the first data structure. Neither is there any language in the cited passages that discloses computing the first source address in the first data structure, where the first source address is equal to the size of a block of memory subtracted from the global address of the write pointer. Thus, *So* does not disclose all of the limitations of claims 8, 18 and 28.

Regarding claims 9, 19 and 29, Applicants respectfully assert that *So* does not disclose "reading said local address of said write pointer; and copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses reading the local address of the write pointer. Neither is there any language in the cited passage that discloses copying the local address of the write pointer. Neither is there any language in the cited passage that discloses copying the local address of the write pointer into an entry in a third data structure located in the first DSP processor core. Thus, *So* does not disclose all of the limitations of claims 9, 19 and 29.

Regarding claims 10, 20 and 30, Applicants respectfully assert that *So* does not disclose "reading a local address of said read pointer; and copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core." The Office Action relies upon column 13, lines 1-23 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. As stated above, *So* instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. *So* further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no

language in the cited passage that discloses reading a local address of the read pointer. Neither is there any language in the cited passage that discloses copying the local address of the read pointer. Neither is there any language in the cited passage that discloses copying the local address of the read pointer into an entry in a third data structure located in the second DSP processor core. Thus, *So* does not disclose all of the limitations of claims 9, 19 and 29.

Regarding claim 21, Applicants respectfully assert that *So* does not disclose "a plurality of digital signal processing (DSP) units." The Office Action has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Office Action must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Office Action has not addressed this limitation, the Office Action has not established a *prima facie* case of anticipation in rejecting claim 21. M.P.E.P. §2131.

Furthermore, regarding claim 21, Applicants respectfully assert that *So* does not disclose "a direct memory access controller coupled to said plurality of DSP processor cores." The Office Action relies upon element 316 in Figure 3 of *So* as disclosing the above-cited claim limitation. Applicants respectfully traverse. Element 316 in Figure 3 of *So* does disclose a DMA control circuit. However, element 316 of *So* is not coupled to a plurality of DSP processor cores. Thus, *So* does not disclose all of the limitations of claim 21.

Additionally, regarding claim 21, Applicants respectfully assert that *So* does not disclose "wherein said direct memory access controller comprises: a memory unit operable for storing a computer program for facilitating inter-DSP data communications; and a processor coupled to said memory unit, wherein said processor, responsive to said computer program." As stated above, the Office Action relies upon element 316 in Figure 3 of *So* as disclosing a direct memory access controller. However, the Office Action now relies upon elements 102, 104, 112 of Figure 2 and column 9, lines 51-62 of *So* as disclosing the above-cited claim

limitation. Elements 102, 104, 112 relate to a CPU, a cache and memory of a personal computer and not to a memory unit and processor of a direct memory access controller (which the Office Action asserts as being disclosed by element 316 in Figure 3 of So). Thus, *So* does not disclose all of the limitations of claim 21.

As a result of the foregoing, Applicants respectfully assert that each and every claim limitation is not found within *So*, and thus claims 1-30 are not anticipated by *So*.

## II. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-30 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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